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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,997	06/30/2003	Hirofumi Nakagawa	60188-449	8190

7590 09/01/2005

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,997	NAKAGAWA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,11 and 14-24* is/are rejected.

7)☒ Claim(s) *8,10 and 12-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4, 6-7, 9, 11 and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka (US 6,924,782) in view of Taguma et al. (JP 11-095729).

Regarding claim 1, Fujioka discloses a display device driving circuit for use with a display device having a display section including sub-pixels arranged in a matrix pattern (Figure 3, items IT01) and a plurality of signal lines for supplying image-forming signals to the sub-pixels (Figure 3, items D), the display device driving circuit comprising: voltage supply lines for transferring the image-forming signals to the plurality of signal lines (Figure 7, items HV and LV); switches for turning ON/OFF the transfer of the image-forming signals to the voltage supply lines (Figure 7, items PM1, NM2, PM2 and

NM1). Fujioka fails to teach of a display device driving circuit comprising shorting means for electrically shorting one of the voltage supply lines that is connected to an odd-numbered one of the plurality of signal lines with another one of the voltage supply lines that is connected to an even-numbered one of the plurality of signal lines during a predetermined period including a period during which the switches are OFF, wherein the shorting means can be turned OFF autonomously when a polarity of a potential of the voltage supply line connected to the odd-numbered signal line and a polarity of a potential of the voltage supply line connected to the even-numbered signal line are switched around. Taguma et al. disclose a display device driving circuit comprising shorting means (Drawing 1, item 30) for electrically shorting one of the voltage supply lines that is connected to an odd-numbered one of the plurality of signal lines (Drawing 1, item 26L) with another one of the voltage supply lines that is connected to an even-numbered one of the plurality of signal lines (Drawing 1, item 26R) during a predetermined period including a period during which the switches are OFF, wherein the shorting means can be turned OFF autonomously when a polarity of a potential of the voltage supply line connected to the odd-numbered signal line and a polarity of a potential of the voltage supply line connected to the even-numbered signal line are switched around (Paragraph [0220]. The examiner interprets this to mean that during switch over, polarity inversion, as shown in Drawing 1, items 24L and 24R, the switches located in 24L and 24R and not connected to a supply line, i.e. the switches are open and that is when the short circuit switch 30 is closed.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and

Taguma et al. in order to provide a display device driving circuit that reduces the power consumption of a display device.

Regarding claim 2, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Taguma et al. also disclose wherein the odd-numbered signal line (Drawing 1, item 26L) and the even-numbered signal line (Drawing 1, item 26R) are adjacent to each other (Drawing 1, items 26L and 26R are next to each other). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce the power consumption of the display device while also allowing for easily connecting parts of the circuit.

Regarding claim 3, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Taguma et al. also disclose wherein the voltage supply lines are all electrically shorted together during the predetermined period (Paragraph [0230] where it states: "...switching means by which said short-circuiting means was connected among all signal lines..."). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and also provide for easier wiring means.

Regarding claim 4, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Fujioka also discloses wherein: the sub-pixels include groups of sub-pixels for different colors to be displayed (Figure 3, items IT01) and the voltage supply line connected to the odd-numbered signal line and the voltage supply line connected to

the even-numbered signal line supply the image-forming signals for driving the sub-pixels of the same color (Figure 7, Y_n and Y_{n+3} represent the signal lines that connect to the odd and even-numbered signal lines respectively and as seen in Figure 3, every Y_n and Y_{n+3} signal line corresponds to the same color). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and connect pixel of the same color together since pixels of the same colors usually have similar characteristics as opposed to pixels of opposite colors, which would provide for an improved display.

Regarding claim 6, Fujioka and Taguma et al. disclose the display device driving circuit of claim 4. Taguma et al. also disclose wherein voltage supply lines that are for supplying the image-forming signals to the sub-pixels of the same color are all electrically shorted together during the predetermined period (Paragraph [0230] where it states: "...switching means by which said short-circuiting means was connected among all signal lines..." The examiner interprets this to mean that if all of the lines are shorted together that the sub-pixels of the same color are then all electrically shorted together.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and also provide for easier wiring means.

Regarding claim 7, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Taguma et al. disclose wherein the shorting means includes: a shorting line for electrically connecting the voltage supply line connected to the odd-

numbered signal line to the voltage supply line connected to the even-numbered signal line during the predetermined period (Drawing 1 shows a shorting line connected to the odd and even-numbered signal lines); a switching element provided along the shorting line (Drawing 1, item 30) and including a control section (Drawing 1, item 32). Fujioka discloses a control element (Figure 7, ENB and M) for performing a control so that either the potential of the voltage supply line connected to the odd-numbered signal line or the potential of the voltage supply line connected to the even-numbered signal Line is applied to the control section at least during the predetermined period (Table 1 in column 11 shows that depending on the values of ENB and M, either the HV signal line, even-numbered signal line, or the LV, odd-numbered signal line, will provide its potential to the outputs. The examiner interprets that since either the odd or even can be provided to the signal lines of Figure 7, that when combined with the control section that is provided in drawing 1 of Taguma et al. that only one of these values would be provided to the control section.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma in order to provide a display device driving circuit that would further reduce the power consumption of the display device.

Regarding claim 9, Fujioka and Taguma et al. disclose the display device driving circuit of claim 7. Taguma et al. also discloses wherein: a polarity of each of the image-forming signals is inverted for every horizontal scanning period (Drawing 1, items 24L and 24R contain switches which invert the polarities of the signal lines every horizontal scanning period as discussed in paragraph [0660]. Fujioka discloses a control is

performed so that either the potential of the voltage supply line connected to the odd-numbered signal line or the potential of the voltage supply line connected to the even-numbered signal line is applied to the control section of the switching element throughout the horizontal scanning period (Table 1 in column 11 shows that depending on the values of ENB and M, either the HV signal line, even-numbered signal line, or the LV, odd-numbered signal line, will provide its potential to the outputs. The examiner interprets that since either the odd or even can be provided to the signal lines of Figure 7, that when combined with the control section that is provided in drawing 1 of Taguma et al. that only one of these values would be provided to the control section of which controls the switching element, item 30.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma in order to provide a display device driving circuit that would further reduce the power consumption of the display device.

Regarding claim 11, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Fujioka also discloses wherein the shorting means includes: a first shorting line (Figure 7, PM2) and a second shorting line (Figure 7, NM2) for electrically connecting the voltage supply line connected to the odd-numbered signal line to the voltage supply line connected to the even-numbered signal line during the predetermined period (Figure 7, PM2 and NM2 each connect the Y_n line, the odd-numbered signal line, to the Y_{n-3} line, the even-numbered signal line, which both can electrically connect the two signal lines together during the time in which ENB is high level, the predetermined period.); a first switching element provided along the first

shorting line (figure 7, PM2), wherein the first switching element is turned ON only when the potential of the voltage supply line connected to the odd-numbered signal line is equal to or greater than the potential of the voltage supply line connected to the even-numbered signal line, and is turned OFF autonomously when the potential of the voltage supply line connected to the odd-numbered signal line is less than the potential of the voltage supply line connected to the even-numbered signal line (Referring to Figure 7, the switches PM2 and NM2 are controlled by ENB and M. Since ENB only determined whether all the switches are OFF/ON, M determines whether PM2 is OFF/ON during the predetermined amount of time. Since M is a conversion-to-AC signal, column 8, lines 14-15, the examiner interprets that since when M is high PM2 is ON and when M is low PM2 is OFF, Table 1 in column 11, that since the odd-numbered signal line is the HV line that M being high means that the potential of HV is considered greater than the LV, even-number signal line and the HV is supplied by turning PM2 ON. Therefore when M is low the potential of the even-numbered signal line is considered greater and PM2 is OFF.); and a second switching element provided along the second shorting line (Figure 7, NM2), wherein the second switching element is turned ON only when the potential of the voltage supply line connected to the even-numbered signal line is equal to or greater than the potential of the voltage supply line connected to the odd-numbered signal line, and is turned 0& autonomously when the potential of the voltage supply line connected to the even- numbered signal line is less than the potential of the voltage supply line connected to the odd-numbered signal line (Referring to figure 7,the concept is the same as mentioned above. Since when M is

high NM2 is OFF and when M is low NM2 is ON, the examiner interprets this to mean that when M is low, the potential of the LV line, the even-numbered signal line, is considered to be greater than the HV line, the odd-numbered signal line, and NM2 is turned ON. Therefore when M is high the potential of the LV line is considered to be less than that of the HV line and NM2 is turned OFF.). Therefore is would have been obvious to "one of ordinary skill" in the art to combine the teaching of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce the power consumption of the display device.

Regarding claim 16, Fujioka and Taguma et al. disclose the display device driving circuit of claim 4. Fujioka also discloses wherein: the display device driving circuit further comprises a plurality of operational amplifiers arranged in a row for transferring the image-forming signals to the switches (Figure 7, HV and LV are operational amplifiers that are arranged in a row as shown in Figure 6.); and one of the plurality of operational amplifiers that is for outputting the image-forming signal to be supplied to the K^{th} signal line is adjacent to another one of the plurality of operational amplifiers that is for outputting the image-forming signal to be supplied to the $(K+3)^{th}$ signal line (Figure 7 shows the HV and LV operational amplifier next to each other of which the HV line is connected to the Y_n signal line and the LV line is connected to the Y_{n-3} signal line.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and connect the signal lines of the same color together since pixels of the same colors usually have similar

characteristics as opposed to pixels of opposite colors, which would provide for an improved display and also to arrange the lines connected together next to each other to provide for better wiring of the circuit.

Regarding claim 17, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Taguma et al. also disclose wherein a polarity of the image-forming signals to be supplied to the odd-numbered signal line is opposite to that of the image-forming signals to be supplied to the even-numbered signal line (Paragraph [0650]). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that reduces power consumption of a driving circuit using an inversion method.

Regarding claim 18, Fujioka discloses a display device driving circuit for use with a display device having a display section including sub-pixels arranged in a matrix pattern (Figure 3, items IT01) and a plurality of signal lines for supplying image-forming signals to the sub-pixels (Figure 3, items D), the display device driving circuit comprising: voltage supply lines for transferring the image-forming signals to the plurality of signal lines (Figure 7, items HV and LV); switches for turning ON/OFF the transfer of the image-forming signals to the voltage supply lines (Figure 7, items PM1, NM2, PM2 and NM1); a plurality of operational amplifiers arranged in a row for transferring image-forming signals to the switches (Figure 7, HV and LV are operational amplifiers that are arranged in a row as shown in Figure 6.), wherein one of the operational amplifiers that is for outputting the image-forming signal to be supplied to

the K^{th} signal line is adjacent to another one of the operational amplifiers that is for outputting the image-forming signal to be supplied to the $(K+3)^{th}$ signal line, where K is a natural number (Figure 7 shows the HV and LV operational amplifier next to each other of which the HV line is connected to the Y_n signal line and the LV line is connected to the Y_{n-3} signal line.). Fujioka fails to teach of a display device driving circuit comprising means for electrically shorting one of the voltage supply lines that is connected to an odd-numbered one of the plurality of signal lines with another one of the voltage supply lines that is connected to an even-numbered one of the plurality of signal lines during a predetermined period including a period during which the switches are OFF. Taguma et al. disclose a display device driving circuit comprising means for electrically shorting (Drawing 1, item 30) one of the voltage supply lines that is connected to an odd-numbered one of the plurality of signal lines (Drawing 1, item 26L) with another one of the voltage supply lines that is connected to an even-numbered one of the plurality of signal lines (Drawing 1, item 26R) during a predetermined period including a period during which the switches are OFF (Paragraph [0220]. The examiner interprets this to mean that during switch over, polarity inversion, as shown in Drawing 1, items 24L and 24R, the switches located in 24L and 24R and not connected to a supply line, i.e. the switches are open, OFF, and that is when the short circuit switch 30 is closed, shorted.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide for reduced power consumption and also to arrange the lines connected together next to each other to provide for better wiring of the circuit.

Regarding claim 19, Fujioka and Taguma et al. disclose the display device driving circuit of claim 18. Taguma et al. also disclose wherein voltage supply lines that are for supplying the image-forming signals to the sub-pixels of the same color are all electrically shorted together during the predetermined period (Paragraph [0230] where it states: "...switching means by which said short-circuiting means was connected among all signal lines..." The examiner interprets this to mean that if all of the lines are shorted together that the sub-pixels of the same color are then all electrically shorted together.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and also provide for easier wiring means.

Regarding claim 20, Fujioka discloses a display device, comprising: a display section, the display section including sub-pixels arranged in a matrix pattern (Figure 3, items IT01), a plurality of signal lines for supplying image-forming signals to the sub-pixels (Figure 3, items D), and a display device driving circuit provided along a frame portion of the display section (Figure 1 shows the driving section along the frame portion of the display section) and including a first voltage supply line connected to the first signal line (Figure 6, Y1, a first signal line, is connected to a low voltage amplifier, a first voltage supply.) and a second voltage supply line connected to the second signal line (Figure 6, Y2, a second signal line, is connected to a high voltage amplifier, a second voltage supply.). Fujioka fails to teach of a display device driving circuit including shorting means for electrically shorting a first, odd-numbered one of the plurality of signal lines with a second, even-numbered one of the plurality of signal lines during a

predetermined period, wherein the shorting means can be turned OFF autonomously when a potential of a voltage supply line connected to the odd-numbered signal line and a potential of a voltage supply line connected to the even-numbered signal line are switched around. Taguma et al. discloses a display device driving circuit including shorting means (Drawing 1, item 30) for electrically shorting a first, odd-numbered one of the plurality of signal lines (Drawing 1, item 26L) with a second, even-numbered one of the plurality of signal lines (Drawing 1, item 26R) during a predetermined period, wherein the shorting means can be turned OFF autonomously when a potential of a voltage supply line connected to the odd-numbered signal line and a potential of a voltage supply line connected to the even-numbered signal line are switched around (Paragraph [0220]. The examiner interprets this to mean that during switch over, i.e. when the potential is switched around, as shown in Drawing 1, items 24L and 24R, the switches located in 24L and 24R and not connected to a supply line, i.e. the switches are open and that is when the short circuit switch 30 is closed, turned OFF, and that this occurs during a predetermined amount of time provided from the control section, item 32). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that reduces the power consumption of a display device.

Regarding claim 21, Fujioka and Taguma et al. disclose the display device of claim 20. Fujioka also discloses wherein: the sub-pixels include groups of sub-pixels for different colors to be displayed (Figure 3, items IT01); and the first signal line and the second signal line are signal lines for supplying the image-forming signals to the sub-

pixels of the same color (Figure 7, Y_n and Y_{n+3} represent the signal lines that connect to the odd and even-numbered signal lines respectively and as seen in Figure 3, every Y_n and Y_{n+3} signal line corresponds to the same color). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and connect pixel of the same color together since pixels of the same colors usually have similar characteristics as opposed to pixels of opposite colors, which would provide for an improved display.

Regarding claim 22, Fujioka and Taguma et al. disclose the display device of claim 21. Taguma et al. also discloses wherein signal lines that are for supplying the image-forming signals to the sub-pixels of the same color are all electrically shorted together (Paragraph [0230] where it states: "...switching means by which said short-circuiting means was connected among all signal lines..." The examiner interprets this to mean that if all of the lines are shorted together that the sub-pixels of the same color are then all electrically shorted together.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce power consumption and also provide for easier wiring means.

Regarding claim 23, Fujioka and Taguma et al. disclose the display device of claim 20. Taguma et al. disclose wherein the shorting means includes: a shorting line for electrically connecting the odd-numbered signal line to the even-numbered signal line during the predetermined period (Drawing 1 shows a shorting line connected to the

odd and even-numbered signal lines); a switching element provided along the shorting line (Drawing 1, item 30) and including a control section (Drawing 1, item 32). Fujioka discloses a control element (Figure 7, ENB and M) for performing a control so that either the potential of the voltage supply line connected to the odd-numbered signal line or the potential of the voltage supply line connected to the even-numbered signal Line is applied to the control section at least during the predetermined period (Table 1 in column 11 shows that depending on the values of ENB and M, either the HV signal line, even-numbered signal line, or the LV, odd-numbered signal line, will provide its potential to the outputs. The examiner interprets that since either the odd or even can be provided to the signal lines of Figure 7, that when combined with the control section that is provided in drawing 1 of Taguma et al. that only one of these values would be provided to the control section.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka and Taguma in order to provide a display device driving circuit that would further reduce the power consumption of the display device.

Regarding claim 24, Fujioka and Taguma et al. disclose the display device of claim 20. Fujioka also disclose wherein the shorting means includes: a first shorting line (Figure 7, PM2) and a second shorting line (Figure 7, NM2) for electrically connecting the odd-numbered signal line to the even-numbered signal line during the predetermined period (Figure 7, PM2 and NM2 each connect the Y_n line, the odd-numbered signal line, to the Y_{n-3} line, the even-numbered signal line, which both can electrically connect the two signal lines together during the time in which ENB is high

level, the predetermined period.); a first switching element provided along the first shorting line (figure 7, PM2), wherein the first switching element is turned ON only when the potential of the voltage supply line connected to the odd-numbered signal line is equal to or greater than the potential of the voltage supply line connected to the even-numbered signal line, and is turned OFF autonomously when the potential of the voltage supply line connected to the odd-numbered signal line is less than the potential of the voltage supply line connected to the even-numbered signal line (Referring to Figure 7, the switches PM2 and NM2 are controlled by ENB and M. Since ENB only determined whether all the switches are OFF/ON, M determines whether PM2 is OFF/ON during the predetermined amount of time. Since M is a conversion-to-AC signal, column 8, lines 14-15, the examiner interprets that since when M is high PM2 is ON and when M is low PM2 is OFF, Table 1 in column 11, that since the odd-numbered signal line is the HV line that M being high means that the potential of HV is considered greater than the LV, even-number signal line and the HV is supplied by turning PM2 ON. Therefore when M is low the potential of the even-numbered signal line is considered greater and PM2 is OFF.); and a second switching element provided along the second shorting line (Figure 7, NM2), wherein the second switching element is turned ON only when the potential of the voltage supply line connected to the even-numbered signal line is equal to or greater than the potential of the voltage supply line connected to the odd-numbered signal line, and is turned 0& autonomously when the potential of the voltage supply line connected to the even- numbered signal line is less than the potential of the voltage supply line connected to the odd-numbered signal line

(Referring to figure 7,the concept is the same as mentioned above. Since when M is high NM2 is OFF and when M is low NM2 is ON, the examiner interprets this to mean that when M is low, the potential of the LV line, the even-numbered signal line, is considered to be greater than the HV line, the odd-numbered signal line, and NM2 is turned ON. Therefore when M is high the potential of the LV line is considered to be less than that of the HV line and NM2 is turned OFF.). Therefore is would have been obvious to "one of ordinary skill" in the art to combine the teaching of Fujioka and Taguma et al. in order to provide a display device driving circuit that would reduce the power consumption of the display device.

4. Claims 5 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka (US 6,924,782) and Taguma et al. (JP 11-095729) and in further view of Udo et al. (US 2002/0050972).

Regarding claim 5, Fujioka and Taguma et al. disclose the display device driving circuit of claim 4. Fujioka and Taguma et al. fail to teach of a display device driving circuit wherein: the signal lines include three groups of signal lines for red, green and blue; and the K^{th} signal line and the $(K+3)^{th}$ signal line are electrically shorted with each other by the shorting means, where K is any natural number. Udo et al. disclose a display device driving circuit wherein: the signal lines include three groups of signal lines for red, green and blue (Figure 3, R, G and B); and the K^{th} signal line and the $(K+3)^{th}$ signal line are electrically shorted with each other by the shorting means (Figure 3, S1 is the shorting means and is connected between signal line D1 and D4), where K

is any natural number. Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka, Taguma et al. and Udo et al. in order to provide a display device driving circuit that would reduce power consumption and connect pixel of the same color together since pixels of the same colors usually have similar characteristics as opposed to pixels of opposite colors, which would provide for an improved display.

Regarding claim 14, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Fujioka and Taguma et al. fail to teach of a display device wherein: connecting portions of the voltage supply lines for connecting the voltage supply lines to the plurality of signal lines are provided in a plurality of wiring layers. Udo et al. discloses a display device wherein: connecting portions of the voltage supply lines for connecting the voltage supply lines to the plurality of signal lines are provided in a plurality of wiring layers (Figure 3, the voltage supply lines connecting the signal lines for D1, D4, D7 and D10 are provided to the same wiring layer and D2, D5, D8 and D11 are provided on the same wiring layer therefore providing a plurality of wiring layers.); and the connecting portions are provided so that those that are connected to adjacent ones of the plurality of signal lines, or those that are connected to ones of the plurality of signal lines of the same color, are adjacent to each other in the same wiring layer (Figure 3, the voltage supply lines connecting the signal lines for D1, D4, D7 and D10, which correspond to the color red, are provided to the same wiring layer and D2, D5, D8 and D11, which correspond to the color green, are provided on the same wiring layer.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the

teachings of Fujioka, Taguma et al, and Udo et al. in order to provide a display device driving circuit which not only reduces power consumption but also provides easier wiring of the circuit.

Regarding claim 15, Fujioka and Taguma et al. disclose the display device driving circuit of claim 1. Fujioka and Taguma et al. fail to teach of a display device driving circuit wherein: connecting portions of the voltage supply lines for connecting the voltage supply lines to the plurality of signal lines are provided in a plurality of wiring layers; and among the connecting portions, those that are connected to adjacent ones of the plurality of signal lines, or those that are connected to ones of the plurality of signal lines of the same color, are separately provided in a first one of the plurality of wiring layers and in a second one of the plurality of wiring layers, the second wiring layer being immediately above the first wiring layer, and are arranged so as to overlap with each other as viewed from above. Udo et al. disclose a display device driving circuit wherein: connecting portions of the voltage supply lines for connecting the voltage supply lines to the plurality of signal lines are provided in a plurality of wiring layers (Figure 3, the voltage supply lines connecting the signal lines for D1, D4, D7 and D10 are provided to the same wiring layer and D2, D5, D8 and D11 are provided on the same wiring layer therefore providing a plurality of wiring layers.); and among the connecting portions, those that are connected to adjacent ones of the plurality of signal lines, or those that are connected to ones of the plurality of signal lines of the same color, are separately provided in a first one of the plurality of wiring layers and in a second one of the plurality of wiring layers, the second wiring layer being immediately

above the first wiring layer, and are arranged so as to overlap with each other as viewed from above (Figure 3, the voltage supply lines connecting the signal lines for D1, D4, D7 and D10 are provided to the same wiring layer and D2, D5, D8 and D11 are provided on the same wiring layer and can bee seen as to over lap as viewed from above in Figure 3.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of Fujioka, Taguma et al, and Udo et al. in order to provide a display device driving circuit which not only reduces power consumption but also provides easier wiring of the circuit and takes up less space.

Allowable Subject Matter

5. Claims 8, 10 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 8, 10 and 12, the primary reason for allowance of the claims is the inclusion of the limitation of including the configuration of MISFET switching elements relating to the shorting device of which could not be found in the prior art. Regarding claim 13, the primary reason for allowance of the claims is the inclusion of the limitation of including the diodes in the directional manner relating to the shorting device switching element of which could not be found in the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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SS

26 August 2005

REGINA LIANG
PRIMARY EXAMINER